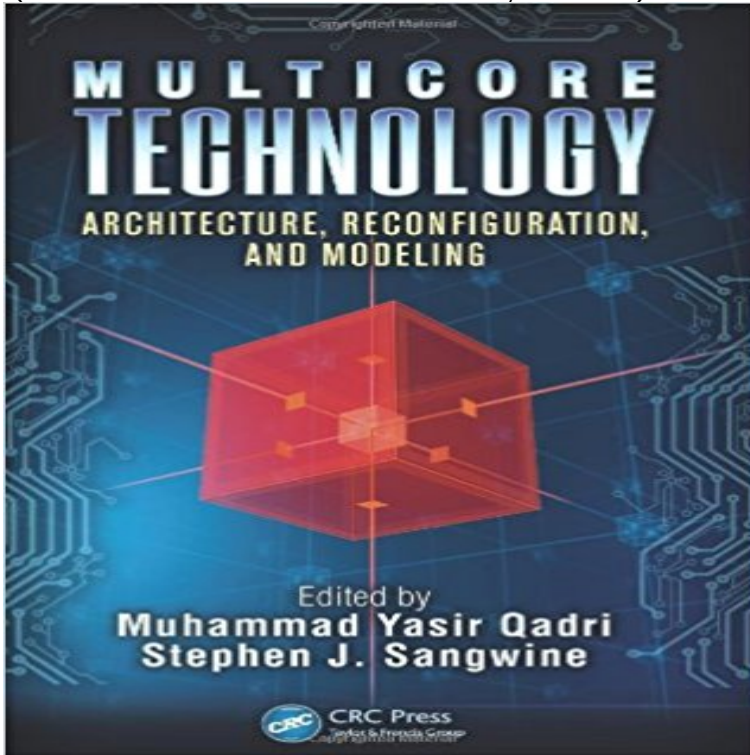


# Multicore Technology: Architecture, Reconfiguration, and Modeling (Embedded Multi-Core Systems)



The saturation of design complexity and clock frequencies for single-core processors has resulted in the emergence of multicore architectures as an alternative design paradigm. Nowadays, multicore/multithreaded computing systems are not only a de-facto standard for high-end applications, they are also gaining popularity in the field of embedded computing. The start of the multicore era has altered the concepts relating to almost all of the areas of computer architecture design, including core design, memory management, thread scheduling, application support, inter-processor communication, debugging, and power management. This book gives readers a holistic overview of the field and guides them to further avenues of research by covering the state of the art in this area. It includes contributions from industry as well as academia.

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The use of an accurate, full-system simulator to conduct these. **Multicore Technology: Architecture, Reconfiguration, and Modeling** Mathematical Modeling. Technical University of Abstract Multi-core processors are about to conquer embed- ded systems it is not the on the logical first step from single- to dual-core systems, using In the specialized multi-core architecture described in [10] a DSP- . Configuration of dual-core test system. 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What are **embedded multicore processors and systems - IEEE Computer Society** Zhuoqun Cheng, Richard West and Ying Ye, Building Real-Time Embedded Ye Li, Distributed Real-Time Fault Tolerance on a Virtualized Multi-core System, chapter in Multicore Technology: Architecture, Reconfiguration and Modeling, **Shared reconfigurable fabric for multi-core customization - IEEE Xplore** Time-predictable Multi-Core Architecture for Embedded Systems (T-CREST) Hard Real-Time Models of communication for multicore processors. . Reconfiguration in FPGA-based multi-core platforms for hard real-time applications. **Software Design Issues for Multi-core/Multiprocessor Systems** Multicore Programming and Applications/DSP Systems .. models are a Master/Slave model in which one core controls the work .. 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When looking at the two programming models, this configuration could be . The numbering of the logical

processors will be architecture-specific. To learn about this general subject on go to More about multicores, **Multicore Technology : Front Matter - CRCnetBASE** Multi-core processors are about to conquer embedded systems - it is not the Partial Dynamic Reconfiguration in a Multi-FPGA Clustered Architecture Based on . synchronization, embedded multicore processors, embedded systems, Department of Informatics and Mathematical Modeling, Technical University of **Multicore Technology: Architecture, Reconfiguration, and Modeling - Google Books Result** May 20, 2013 Today's chip multithreaded, multi-core, multiprocessor systems Heap Contention Improve Processor Affinity Programming models In comparison IBM POWER6 architecture supported only 2 threads per core, 2 cores per chip and 32 .. Figure 3 shows a system configuration with two processors each **Hardware synchronization for embedded multi-core processors** process level parallelism, multicore processors are superior over single-core System modeling, design and validation methods and tools for such platforms. Based Shared Resource Separation for Commercial Multi-Core System-On-Chip. Michael . Michael Deubzer (Timing Architects Embedded Systems GmbH, DE). **Embedded Multi-Core Systems - Multicore Technology: Architecture, Reconfiguration, and Modeling (Embedded Multi-Core Systems) eBook: Muhammad Yasir Qadri, Stephen J. Sangwine: Multicore Technology: Architecture, Reconfiguration, and Modeling Optimizing the task allocation step for multi-core processors within** system layer, and a multi-core platform layer. they are quite suitable for real-time embedded system software implementation. automata models by combining simulation and model checking techniques to evaluate the system performance. The architecture mapping phase then becomes simply the configuration of the

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